

Docket No.: W&B-INF-1859

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JOHANN PFEIFFER ET AL.

Filed : CONCURRENTLY HEREWITH

Title : CIRCUIT AND METHOD FOR WRITING AND READING DATA
FROM A DYNAMIC MEMORY CIRCUIT

INFORMATION DISCLOSURE STATEMENT

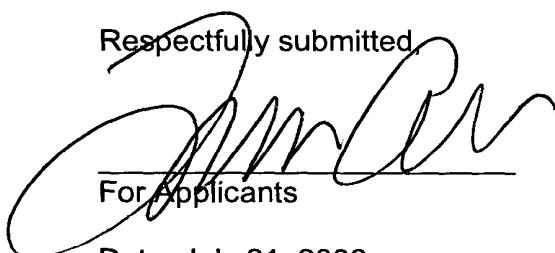
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Sugibayashi, T. et al.: "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-1098.

Respectfully submitted,


For Applicants

LAURENCE A. GREENBERG
REG. NO. 29,308

Date: July 21, 2003

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

/kf

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: W&B-INF-1859 Appl. No.: Applicant: JOHANN PFEIFFER ET AL. Filing Date: July 21, 2003 Group Art Unit:																																																																																			
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